REMARKS

The claims are claims 1 and 7.

The Title of the Invention has been changed to "VERY LONG INSTRUCTION WORD MICROPROCESSOR WITH EXECUTION PACKET SPANNING TWO OR MORE FETCH PACKETS WITH PRE-DISPATCH INSTRUCTION SELECTION FROM TWO LATCHES ACCORDING TO INSTRUCTION BIT." This amended title is properly reflective of the subject matter claimed.

Claim 7 is amended to make clear that the selection is from among a closed set of three outputs.

Claim 7 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Simar et al EPO Published Patent Application No. 0 855 648 and Heishi et al U.S. Patent No. 6,324,639.

Claim 7 recites subject matter not made obvious by the combination of Simar et al and Heishi et al. Claim 7 recites "selecting only one output from among the set consisting of an entire instruction from a predetermined section of said first latch, an entire instruction from a corresponding section of said second latch, and no instruction, dependent upon only said p-bit from each instruction stored in said first latch and each instruction stored in said second latch." This amended language makes the capability of selecting no instruction mandatory. Note that use of the closed language "consisting of" requires selection from the three listed options and only from these three options.

This recitation of claim 7 differs from the teachings of the combination or Simar et al and Heishi et al in several ways. The "selecting only" language of claim 7 differs from the teachings of Heishi et al. Heishi et al fails to teach that his selectors 224a, 224b, 224c and 224d select instructions only from a predetermined section of the first latch and a corresponding section of the second latch. Figure 8 of Heishi et al clearly shows that each selector 224a, 224b, 224c and 224d is connected at all sections A0,

A1, A2 and A3 of instruction buffer A 221 and all sections B0, B1, B2 and B3 of instruction buffer B 222. As a consequence each selector 224a, 224b, 224c and 224d of Figure 8 of Heishi et al requires six inputs, one input from each section A0, A1, A2, A3 of instruction buffer 221 and one input from each section B0, B1, B2 and B3 of instruction buffer 222. In contrast, the selection recited in claim 7 requires only two inputs, one from a single section of latch stage 910 and one from a corresponding single section of latch stage 911. Thus this invention accomplishes a similar purpose using a simpler method. Accordingly, claim 7 is not made obvious by the combination of Simar et al and Heishi et al.

This language of claim 7 differs from the teachings of the combination or Simar et al and Heishi et al in another manner. Claim 7 requires selection of an entire instruction from the first or second latch. Heishi et al teaches a variable length instruction of either 21 bits or of 42 bits. Thus multiplexers 224a, 224b, 224c and 224d of Figure 8 of Heishi et al do not select whole instructions from respective instruction buffers A 221 and instruction buffer B 222. Multiplexers 224a, 224b, 224c and 224d select instead select a predetermined number of bits (21 bits) from one of the sections A0, A1 or A2 of instruction buffer A 221 or sections B0, B1 or B2 of instruction buffer B 22. Heishi et al teaches that these 21 bits may be an entire instruction or may be only part of an instruction. The closed language "consisting of" in claim 7 denies the possibility of selection of part of an instruction. Accordingly, claim 7 is allowable over the combination of Simar et al and Heishi et al.

This language of claim 7 differs from the teachings of the combination or Simar et al and Heishi et al in yet another manner. The combination of Simar et al and Heishi et al fails to make obvious the multiplexer selection of no instruction. The closed language "consisting of" requires selection from the three listed

options and only from these three options. The examples of Heishi et al at column 14, lines 1 to 62 and illustrated in Figures 9A, 9B, 9C, 9D, 9E, 9F, 10A, 10B, 10C, 10D and 10E show that all selectors 224a, 224b, 224c and 224d select an instruction from either instruction buffer A 221 or instruction buffer B 222 each time a selection is made by any of the multiplexers. These selections are illustrated in Figure 9D (column 14, lines 27 to 31), Figure 10A (column 14, lines 44 to 48) and Figure 10D (column 14, lines page 53 to 58). Selectors 224a, 224b, 224c and 224d each select an instruction to be transferred to instruction register 23 even for instances when all such instructions cannot be dispatched. In this application selection of no instruction is the same as a coding of a no operation instruction according to Simar et al and results in no instruction dispatch. Heishi et al states at column 15, lines 27 to 36:

> "The instruction issuing control unit 31 refers to the parallel execution boundary information f10 and the format information f11 of the units stored in the instruction register A231 and the instruction register B232, and judges which is the final unit that should be outputted from the instruction register 23 in this cycle. Based on this information, the instruction issuing control unit 31 outputs control signals (no-operation instruction flags) that show whether the decoding by the second instruction decoder 34 and third instruction decoder 35 should be invalidated."

Thus Heishi et al teaches another structure instruction issuing control unit 31 controlling the issue of no-operation control signals to first instruction decoder 33, second instruction decoder 34 and third instruction decoder 35 than recited in claim 7. Accordingly, claim 7 1s not made obvious by the combination of Simar et al and Heishi et al.

In summary, Heishi et al teaches performing the selection of instructions in a different manner than recited in claim 7. Heishi

et al teaches selectors 224a, 224b, 224c and 224d which determine both the instructions selected and the corresponding functional unit used dependent on their position in the original instruction stream. In contrast, claim 7 recites two method steps, selecting and dispatching. Accordingly, claim 7 achieves a similar purpose to the disclosure in Heishi et al employing different method steps.

Claim 1 has been allowed.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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